REASON FOR ALLOWANCE

1. Claims 1, 3-7, 9-13 are allowed. Claims 2, 8, 14, 15 have been cancelled.

2. The following is an examiner's statement of reason for allowance:

The prior art fails to teach or suggest an electronic circuit, comprising: a shift circuit that shifts j-bit digital data (j is a natural number) to be converted into k-bit digital data (k is a natural number); and a correction circuit that is electrically coupled to the shift circuit, the correction circuit continuously changes the k-bit digital data that is obtained by the shift circuit in accordance with the change of the j-bit data, the k-bit digital data being extended digital data which is larger than the j-bit digital data; and the shift circuit classifying a range of the j-bit digital data into a plurality of groups and shifting the digital data of each group by a predetermined number of bits in accordance with each group to convert it into the k-bit digital data as claimed in claim 1.

The prior art fails to teach or suggest an electro-optical device, comprising: a control circuit that outputs j-bit luminance gray scale data (j is a natural number); a driving circuit that generates analog driving signals based on the j-bit luminance gray scale data; and a pixel circuit that drives current driven elements based on the analog driving signals, the driving circuit including: a shift circuit that shifts the j-bit luminance gray scale data to convert the data into k-bit digital data (k is a natural number); a correction circuit that is electrically coupled to the shift circuit, the correction circuit continuously changing the k-bit digital data that is obtained by the shift circuit in accordance with the change of the j-bit luminance gray scale data, the k-bit digital data being extended digital data that is larger than the j-bit luminance gray scale data; and

the shift circuit classifying a range of the j-bit digital data into a plurality of groups and shifting the digital data of each group by a predetermined number of bits in accordance with each group to convert the digital data into the k-bit digital data as claimed in claim 7.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 571-272-7664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nitin Patel/

Primary Examiner, Art Unit 2629